REMARKS

In response to the pending Office Action, claims 4, 5, 12, 14, 15, and 18 have been amended. Claims 1-3, 6-11, and 13 have been cancelled and claims 20 and 21 have been added. Support for the present amendments and the added claims may be found in the application at, for example, page 11, line 19 to page 17, line 17 and FIGS. 1, 2, and 4.

Rejection under 35 U.S.C. §102(e)

Claims 4, 5, 12 and 14-19 were rejected under 35 U.S.C. §102(b) as being anticipated by Japanese Patent Application Publication Number 08-154253 ("Watanabe"). Claims 4, 5, and 12 are independent. Applicants respectfully traverse this rejection for at least the following reasons.

Claim 4 recites a solid state imaging apparatus including, among other features, a signal output circuit configured to perform one of two types of operations, wherein the signal output circuit includes: a first shift register for sequentially outputting selection signals, which select each pixel, to all of the plurality of the pixels either in a vertical or a horizontal direction and a second shift register for continuously outputting the selection signals to some of the plurality of pixels having color filters of the same color either in a vertical or a horizontal direction partially.

To illustrate, in one aspect, the present invention can make it possible for a signal output circuit to select one of two operations. Hence, according to the present invention, it is possible to switch between a regular operation, in which selection signals selecting each pixel can be sequentially output to all pixels either in a vertical or horizontal direction, and a mixture operation, in which selection signals selecting each pixel can be continuously output to some pixels having color filters of the same color either in a vertical or horizontal direction partially.

Applicants respectfully request reconsideration and withdrawal of the rejection of claim 4 because Watanabe fails to describe or suggest a solid state imaging apparatus including, among other features, a signal output circuit configured to perform one of two types of operations, wherein the signal output circuit includes: a first shift register *for sequentially outputting selection signals, which select each pixel, to all of the plurality of the pixels either in a vertical or a horizontal direction* ***and*** a second shift register *for continuously outputting the selection signals to some of the plurality of pixels having color filters of the same color either in a vertical or a horizontal direction partially*, as embodied in claim 4.

Watanabe, in FIG. 1, discloses a solid state imaging apparatus including plural pixels having four color components (a), (b), (c), and (d) and plural vertical shift registers. Watanabe at Abstract. The plural vertical shift registers in an even numbered column in a storage section (12) are formed to have one bit more than those in an odd numbered column. *Id.* Thus, after the information charge is transferred from the vertical shift registers of an odd numbered column to horizontal shift registers of a horizontal transfer section (13), the information charge is transferred from the vertical shift registers of an even numbered column to the horizontal shift registers of the horizontal transfer section (13).

Apparently, this structure allows the information charge, representing the same color component, to be transferred to and outputted from the horizontal transfer section (13) consecutively. To this end, at best, Watanabe generally describes a solid state imaging apparatus performing a "mixture" operation which continuously outputs pixel signals of the same color by simultaneously operating the vertical shift registers (e.g., alleged first register) of the storage section (12) and the horizontal shift registers of the horizontal transfer section (13) (e.g.,

alleged second shift register). That is, both of the alleged first and second registers of Watanabe are needed to effect the "mixture" operation.

However, Watanabe does not describe or otherwise suggest a solid state imaging apparatus including, among other features, a signal output circuit configured to perform one of two types of operations, wherein the signal output circuit includes: a first shift register *for sequentially outputting selection signals, which select each pixel, to all of the plurality of the pixels either in a vertical or a horizontal direction* ***and*** a second shift register *for continuously outputting the selection signals to some of the plurality of pixels having color filters of the same color either in a vertical or a horizontal direction partially*, as embodied in claim 4. That is, Watanabe relied on portions does not disclose a ***combination*** of two registers enabling two distinct operational modes, and instead discloses only, at best, a register arrangement for effecting the aforementioned "mixture" operation.

Furthermore, in Watanabe, the charge signals of each pixel are transferred through a vertical shift register and a horizontal shift register. In other words, each shift register functions as a transfer line for a charge. In contrast, the shift register of the present invention can be a signal output circuit, outputting selection signals that select each pixel, for controlling the output order of the charge signals of pixels.

For at least the foregoing reasons, Applicants respectfully request that the 102 rejection of claim 4 and its dependent claims be withdrawn.

Claims 5 and 12 include features similar to the above-recited features of claim 4. Therefore, for at least the reasons similar to those presented above with respect to claim 4, Applicants respectfully request that the 102 rejection of claims 5 and 12 be withdrawn.

Dependent Claims

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Because claims 4, 5, and 12 are allowable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also allowable. In addition, it is respectfully submitted that the dependent claims are allowable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are allowable over the cited prior art. Accordingly, it is respectfully requested that the 102 be withdrawn.

Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

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